1. A method to solve via poisoning for insulative porous low-k materials comprising the steps of:

providing a substrate having a first and a second insulative layers separated from each other by an intervening etch-stop layer formed therein said substrate;

forming a hole opening in said first and second insulative layers, including said intervening etch-stop layer;

forming a low-k protection layer over said substrate, including in said hole opening;

forming a trench opening over said hole opening to form a dual damascene structure;

forming a barrier layer on the vertical walls of said trench opening and on said low-k protection layer on the vertical walls of said hole opening;

forming a metal layer over said barrier layer in said dual damascene structure; and

performing chemical mechanical polishing (CMP) to complete the forming dual damascene structure.

2. The method of claim 1, wherein said first insulative layer is a low-k dielectric having a dielectric constant between about 2.0 to 3.0.

3. The method of claim 1, wherein said first insulative layer has a thickness between about 2000 to 100000 Å.

4. The method of claim 1, wherein said intervening etch-stop layer is silicon nitride.

5. The method of claim 1, wherein said intervening etch-stop layer has a thickness between about 50 to 1000 Å.

6. The method of claim 1, wherein said second insulative layer is a low-k dielectric having a dielectric constant between about 2.0 to 3.0.

7. The method of claim 1, wherein said second insulative layer has a thickness between about 2000 to 100000 Å.

8. The method of claim 1, wherein said low-k protection layer comprises SiO_2, SiN, SiC and SiNC.

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9. The method of claim 1, wherein said low-k protection layer has a thickness between about 20 to 1000 Å.

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10. The method of claim 1, wherein said barrier layer comprises Ta, Ti, TaN, TiSiN, TaSiN, WN.

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11. The method of claim 1, wherein said barrier layer has a thickness between about 30 to 500 Å.

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12. The method of claim 1, wherein said metal comprises copper.

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13.A method to solve via poisoning for insulative porous low-k materials comprising the steps of:

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providing a substrate having a passivation layer formed over a first metal layer formed on said substrate;

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forming a first insulative layer over said substrate;

forming an etch-stop layer over said first insulative layer;

forming a second insulative layer over said etch-stop layer;

forming a first photoresist layer over said second insulative layer and patterning said photoresist to form a first photoresist mask having a hole pattern;

etching said first and second insulative layers, including said etch-stop layer through said hole pattern to form a hole reaching said passivation layer;

removing said first photoresist mask;

forming a low-k protection layer over said substrate, including in said hole opening;

forming a second photoresist layer over said substrate, including said hole opening and patterning said second photoresist to form a second photoresist mask having a trench pattern;

etching said second insulative layer through said trench pattern in said second photoresist mask to form a trench in said second insulative layer, thus completing the forming of said dual damascene structure in said substrate;

removing said second photoresist mask;

removing said low-k protection layer from over said substrate and from the bottom of said hole opening and thereby exposing underlying said passivation layer while leaving said low-k protection layer on the vertical sides of said hole opening;

removing said passivation layer from said bottom of said hole opening, thereby exposing underlying said first metal layer;

forming a barrier layer over said substrate, including in said dual damascene structure;

depositing a second metal over said barrier layer in said dual damascene structure; and

performing chemical mechanical polishing (CMP) to complete the forming of said dual damascene structure.

14. The method of claim 13, wherein said substrate is silicon.

15. The method of claim 13, wherein said passivation layer comprises silicon nitride (SiN).

16. The method of claim 13, wherein said passivation layer has a thickness between about 30 to 1000 Å.

17. The method of claim 13, wherein said first insulative layer is a low-k dielectric having a dielectric constant between about 2.0 to 3.0.

18. The method of claim 13, wherein said first insulative layer has a thickness between about 2000 to 100000 Å.

19. The method of claim 13, wherein said intervening etch-stop layer is silicon nitride.

20. The method of claim 13, wherein said intervening etch-stop layer has a thickness between about 30 to 1000 Å.

21.The method of claim 13, wherein said second insulative layer is a low-k dielectric having a dielectric constant between about 2.0 to 3.0.

22.The method of claim 13, wherein said second insulative layer has a thickness between about 2000 to 100000 Å.

23. The method of claim 13, wherein said etching said first and second insulative layers is accomplished with a recipe comprising C_2F_6, C_4F_8, Ar, N_2 and O_2.

24. The method of claim 13, wherein said etching said etch-stop layer is accomplished with a recipe comprising C_2F_6, C_4F_8, Ar, N_2 and O_2.

25.The method of claim 13, wherein said low-k protection layer comprises SiO_2, SiN, SiCN and SiC.

26.The method of claim 13, wherein said low-k protection layer has a thickness between about 30 to 1000 Å.

27. The method of claim 13, wherein said removing said low-k protection layer is accomplished with a recipe comprising C_2F_6, C_4F_8, Ar, N_2 and O_2.

28. The method of claim 13, wherein said barrier layer comprises Ta, Ti, TaN, TiSiN, TaSiN, WN.

29. The method of claim 13, wherein said barrier layer has a thickness between about 30 to 500 Å.

30. The method of claim 13, wherein said second metal comprises copper.

31. A damascene structure with a protection layer for low-k materials comprising:

a substrate having a damascene structure with an upper trench opening and a lower hole opening formed in a low-k dielectric layer;

a low-k protection layer on the vertical walls of said lower hole opening;

a barrier layer over said low-k protection layer on said

vertical walls of said lower hole opening, and on the vertical walls of said trench opening; and

a metal layer deposited in said dual damascene structure.

32. The damascene structure of claim 31, wherein said low-k dielectric layer comprises black diamond, CVD SiC, SiLK, polymer.

33. The damascene structure of claim 31, wherein said low-k protection layer comprises SiO_2, SiN, SiC and SiCN.